What is claimed is:

1. A method for checking layout accuracy in an integrated circuit design, comprising:

creating a schematic;

adding a line width marker to selected lines having a width greater than an absolute minimum width;

assigning a line width to each line width marker;

creating a layout;

checking the layout versus the schematic;

extracting a design from the layout, the design having a design line width corresponding to each line having a line width marker; and

checking the design line width versus marker line width for each line having a line width marker.

2. The method of claim 1, wherein checking the design line width further comprises excluding a predetermined area around and above any transistors in the design.

3. The method of claim 1, and further comprising integrating the line width marker into the layout.

4. The method of claim 1, and further comprising locating the line width marker in the schematic.

5. The method of claim 1, wherein creating the layout comprises creating the layout from the schematic.

6. The method of claim 1, wherein creating the layout comprises drawing the layout as specified by the line width assigned to each line width marker.

7. The method of claim 1, and further comprising generating an error condition when a design line width is less than a marker line width.

8. The method of claim 1, and further comprising checking lines without line width markers for the absolute minimum width.

9. The method of claim 1, wherein the lines having a width greater than the absolute minimum width comprise lines for carrying power to transistors in the design.

10. A method for checking layout accuracy in an integrated circuit design, comprising:

creating a schematic;

adding a line width marker to selected lines in the schematic having a width greater than an absolute minimum width;

assigning a line width parameter to each line width marker;

creating a layout from the schematic, the layout having a layout line width for each line in the schematic having a line width marker;

comparing the layout line widths to corresponding line width parameters;

extracting a design from the layout, the design having a design line width for each line in the schematic having a line width marker; and

checking the design line width versus line width parameter for each line in the schematic having a line width marker.

11. The method of claim 10, wherein checking the design line width further comprises excluding a predetermined area around and above any transistors in the design.

12. The method of claim 10, wherein creating the layout further comprises drawing the layout as specified by the line width parameters.

13. The method of claim 10, and further comprising generating an error condition when a design line width is less than a corresponding line width parameter.

14. The method of claim 10, and further comprising checking lines without line width markers for the absolute minimum width.

15. The method of claim 10, wherein extracting a design from the layout is performed when the layout line widths are greater than or equal to the corresponding line width parameters.

16. The method of claim 10, and further comprising generating an error condition when a layout line width is less than a corresponding line width parameter.

17. A method for checking layout accuracy in an integrated circuit design, comprising:

creating a schematic;

adding a line width marker to selected lines in the schematic having a width greater than an absolute minimum width;

assigning a line width parameter to each line width marker;

creating a layout from the schematic, the layout having a layout line width corresponding to each line in the schematic having a line width marker;

comparing the layout line widths to corresponding line width parameters;

generating a first error condition when a layout line width is less than a corresponding line width parameter;

when the layout line widths are greater than or equal to the corresponding line width parameters, extracting a design from the layout, the design having a design line width corresponding to each line in the schematic having a line width marker;

checking the design line width versus line width parameter for each line in the schematic having a line width marker; and

generating a second error condition when a design line width is less than a corresponding line width parameter.

18. The method of claim 17, and further comprising indicating or recording at least one of the first and second error conditions.

19. The method of claim 17, wherein checking the design line width further comprises excluding a predetermined area around and above any transistors in the design.

20. The method of claim 17, wherein creating the layout further comprises drawing the layout as specified by the line width parameters.